REMARKS

In response to the outstanding Office Action:

Specification. The title is amended as required.

§ 102. Claims 1 and 12 were rejected over Maruyama '684. This rejection is believed to be moot in view of the present amendment, whereby a feature of claim 2 (the passive element) is now recited in claim 1.

§ 103. Claims 2-11, 13, and 14 were rejected over Maruyama in view of Aoki '086. This rejection is respectfully traversed.

Amended claim 1 now recites a passive element (more specifically recited in claims 3 and 5 as comprising a capacitor or inductor) located in the wiring region (112 in Fig. 2) that surrounds the circuit region (111 in Fig. 2). This feature is exemplified by elements 260 or 270 in Fig. 2.

The Applicant's specification at page 2, line 15 to page 3, line 2, explains that a problem exists in the prior art, namely, the problem of double design for chips intended for WCSP and chips intended for wire-bonding.

The Applicant's wiring region might be used with one type of structure (e.g., WCSP) but might not be needed with another (e.g., wire bonding); however, the same *chip circuit* design might be adaptable to both connection structures. The Applicant increases efficiency by reducing the number of circuit designs needed by adapting the design for either (e.g.) WCSP or wire-bonding, making the wiring region such that it can be cut away from the circuit region or not, depending of the connection structure used, and, at the same time, putting needed passive elements only in the wiring region. The Examiner is referred to page 25, line 24 through page 26, line 6 of the instant specification.

If a passive element needed for the second redistribution wiring is located in the outer wiring region, then in the case that the wiring region is not needed and is cut away, the passive element is also cut away. If, on the other hand, the same passive element were disposed over the circuit region, it would remain when the wiring region were cut away, and would constitute and unnecessary portion of the circuit requiring a larger and more expensive circuit region.

Therefore, by putting the passive element in the wiring region, the Applicant has advanced the art, not only allowing one circuit design for different connection types but also making that circuit design more efficient. This is not disclosed or suggested by the applied art.

Maruyama discloses a chip with terminals of two types, testing and non-testing. The testing terminals, such as terminal 13A in Fig. 1, are distinct from the non-testing terminals such as terminals 14 and 13B (col. 7, lines 18-28 and 36-38). All of the non-testing terminals are located in the circuit region. The testing terminals 16 are, conversely, located outside the circuit region 12 in the outer region 18. They are connected to the circuit region by traces 15 (col. 7, lines 43-57), which extend outside the circuit region 12 to the outer region 18 (col. 8, lines 56-49).

Maruyama writes, at col. 8, line 49, that "when the wafer level package 10A is used as individualized semiconductor devices 40 [i.e., after testing] .... The test terminals 16 are provided on the positions to be scribed (i.e. scribe regions). In Fig. 3, the scribe regions are indicated by dash-dot lines." At col. 18, line 1, Maruyama further explains, "As shown in FIG. 19, in the cutting process, the outer region 18 is cut and removed by a dicing saw 39. Thus, individualized semiconductor devices 40 are formed. The cutting positions [are] shown by the dot-dash line shown in FIG. 3.... the size of the semiconductor device 40 viewed from above will be approximately equal to the size of the circuit region 12." It appears that the dash-dot lines in Fig.

3 show the center of the saw cut, but because of the width of the saw blade (shown in Fig. 19), the outer region 18 is entirely removed.

Here Maruyama actively teaches that the outer (wiring) region, which is useless after completion of the testing which is Maruyama's concern, should be removed.

The Examiner admits that Maruyama does not disclose a passive element in a wiring region, and relies on Aoki for disclosing this feature.

Aoki discloses an LC circuit in applied Figs. 15A-15C. Feature 1 in these figures is a semiconductor substrate with "elements formed in an integrated manner within the circuit element forming region DA" (¶ [0036]). In other words, feature 1 is an integrated circuit chip with circuits inside the region bordered by line DA, which is shown in Figs. 2-3. It is clear from those figures that both the posts 6 and the connection pads 2 are within the line DA and therefore within the circuit region. There is no disclosure of traces extending beyond the border of the circuit region.

Aoki teaches that all connections to the chip are through the surface, to the wiring board 30 shown in the applied figures. Aoki writes, "a wiring board 30 bearing a plurality of wiring patterns [couples to] the semiconductor device 200 [which] is mounted on the wiring board 30 ... via the solder balls B formed on the posts 6" (¶ [0067]). The description of applied Figs. 15A-15C (in ¶¶ [0072]-[0076]) is similar.

Combination. In summary of the above, one applied reference (Maruyama) discloses no passive devices, and teaches that the wiring region is always removed after testing. The other reference (Aoki) teaches a passive device located in a circuit region, and discloses no wiring region. The Examiner is invited to consider:

(1) No possible combination of these references (not admitted obvious to combine) would produce a passive device in a wiring region, because neither one discloses a passive device in a wiring region.

(2) Aoki teaches (¶ [0080]) that passive circuits should not be "outside the chip," and therefore teaches against putting passive devices onto a wiring region like the outside region 18 of Maruyama.

(3) Even if, for argument's sake, a passive device in a wiring region *were* produced from the prior art (not admitted), the applied art as a whole teaches that it should be discarded after testing, because the sole reference to disclose an outer region also teaches discarding that region prior to use; the finished chip would lack the passive elements. The teaching of the art "as a whole" must be considered under § 103(a) and MPEP § 2141.

(4) Neither reference mentions the problem solved by the Applicant, namely the cost of double design for WCSP and wire-bond chips (page 2, line 15 to page 3, line 2). Therefore, the person of ordinary skill in the art would not have been motivated to solve this problem from the applied prior art, and still less would have been guided to the Applicant's advance.

(5) The Examiner asserts that combination would have been obvious to provide an antenna or signal filtering to Maruyama.

With respect, Maruyama itself does not suggest any need for an antenna or signal filtering, and the Applicant believes that an antenna structure would interfere with Maruyama's testing by leaking energy and causing cross-talk, while filtering would be useless since the testing would probably take place at a definite clock frequency.

The other reference, Aoki, teaches against antennae in ¶ [0080].

(6) Neither reference discloses the claimed redistribution wiring. One teaches solder balls, the other only connection to test equipment.

§ 103. Claims 15, 16, 18, 19, 21, and 22 were rejected over Maruyama in view of Aoki '086. This rejection is respectfully traversed on the same grounds as set out above.

New claim 23 is patentable for the reasons set out above and its dependence, as well as the fact that its subject matter is not seen in either of the applied references.

Allowability of claims 17 and 20 is acknowledged with appreciation. Allowance of the remaining claims is solicited on the basis of the arguments and amendments above.

Respectfully submitted,

March 7, 2005
Date

Nick Bromer (Reg. No. 33,478)
RABIN & BERDO, P.C.
CUSTOMER NO. 23995
Telephone: (202) 371-8976
Telefax : (202) 408-0924